Quectel Cellular Engine

GSM UART Port Application Notes

GSM_UART_AN_V1.00

Document Title	GSM UART Port Application Notes
Version	1.00
Date	2009-06-26
Status	Release
Document Control ID	GSM_UART_AN_V1.00

General Notes

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0. Revision history

Revision	Date	Author	Description of change
1.00	2009-06-25	Jay XIN / Ken JI	Initial

1. Introduction

This document describes the UART port of Quectel GSM module and how to use it in customer's application design. This document can help you quickly understand the UART port of the module.
Note: AT command can be input through UART port only after module is powered on and the Unsolicited Result Code "RDY" is output.

2. Connection

Data Terminal Equipment (DTE) communicates with the module through its main UART port. The voltage level of UART port interface is 2.8 Volts. If the voltage level of DTE's UART pins doesn't match with the module, level shifter circuit should be inserted. ,

The UART pins include TX data (TXD), RX data (RXD), Request To Send (RTS), Clear To Send (CTS), Data Terminal Ready (DTR). Data Carrier Detect (DCD) and Ring Indicator (RI). Not all UART pins are necessary in customer's application. If the module is used as a modem, all pins are needed. The modem control signal RI can be used to indicate to the DTE that a call or Unsolicited Result Code (URC) is received. Hardware handshake using the RTS and CTS signals and XON/XOFF software flow control are both supported.

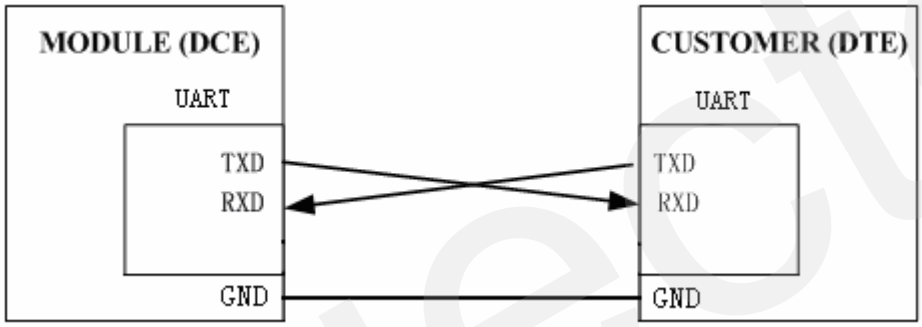

Figure 1: Connecting TXD and RXD

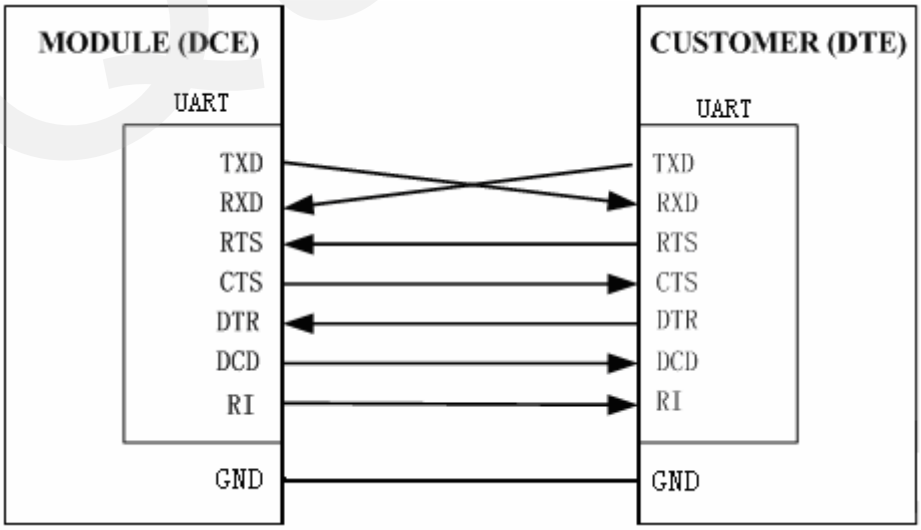

Figure 2: Connecting all signals

3. Level Shifter

Normally, the voltage of VDD_EXT is 2.8V and the DC characteristics of UART port are listed in Table 3.

Table 1: Logic levels of the UART port

Symbol	MIN	MAX	Unit
V_{IL}	0	0.67	V
V_{IH}	1.7	VDD_EXT+0.3	V
V_{OL}	0	0.34	V
V_{OH}	2.0	VDD_EXT	V

NOTE: If the voltage level of UART pins in DTE and the module doesn't match with each other, level shifter circuit should be inserted.

3.1. Communicate with DTE

It is recommended to design the level shift circuit by choosing open drain output buffer (e.g. NC7WZ07) or discrete transistor.

Note:VDD_EXT is supplied by the module(2.8V). VCC_MCU is the voltage for host MCU UART interface.

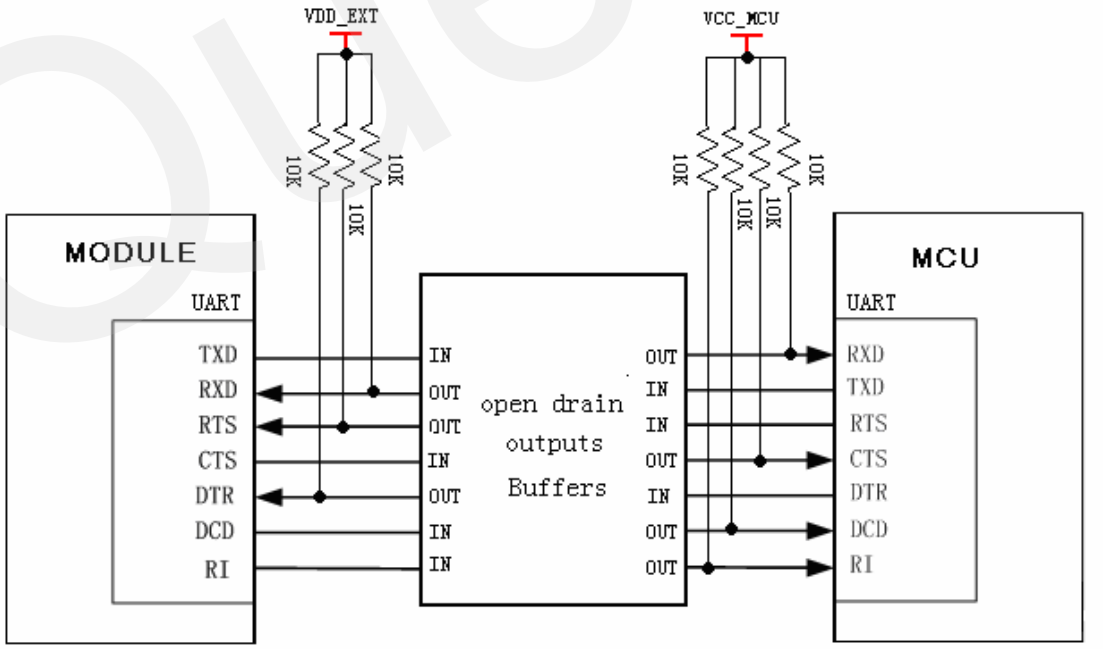

Figure 3: The reference level shifter by using open drain output buffer

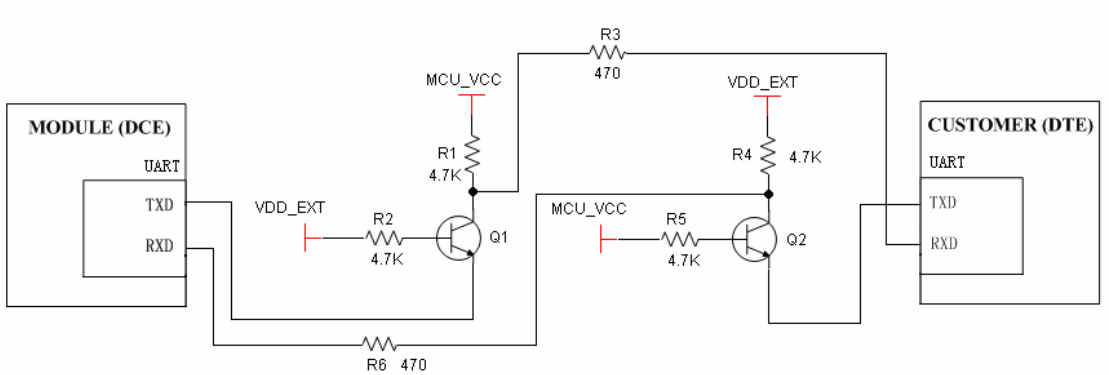

Figure 4:The reference level shifter by using bipolar transistor

3.2. Communicate with the RS-232 port of PC

Table 2:The voltage of RS-232

Logic level	Transmitter capable	Receiver capable	Unit
Logic 0	+5~+15	+3~+25	V
Logic 1	-5~-15	-3~-25	V
Undefined		-3~+3	V

It is suggested to design the level shifter by using RS-232 transceivers, e.g. SP3238E or MAX3221.

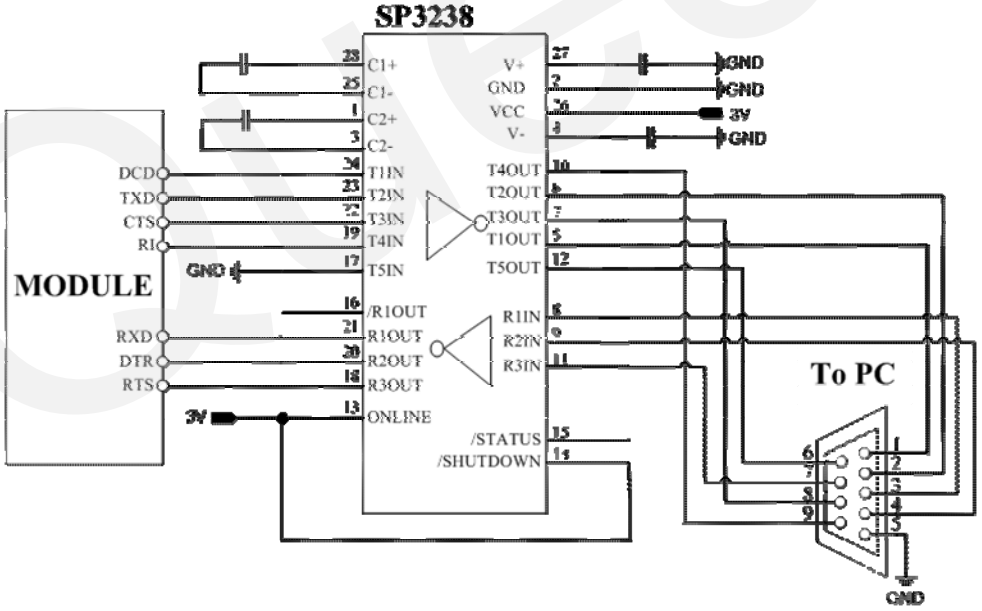

Figure 5:The reference level shifter by using SP3238E for communicating with PC

If only the RXD and TXD pins need to be connected, MAX3221 could be chosen for the level shifter.

4. Firmware Upgrade

To upgrade module firmware in the future, it is strongly recommended to reserve a connector of 4-pin (RXD, TXD, PWRKEY, GND).

NOTE:

1. Please reserve a 4-pin connector on customer's board for firmware upgrade.
2. The PWRKEY can be used to power cycle the module when there is no other method to do this, which is necessary for firmware upgrade.
3. The RS-232 transceiver (e.g. SP3238E) on the upgrade board should be powered by a +3V power supply.
4. R2 is a 2.2KΩ resistor on the customer's host board which is used to prevent the data corruptions when the module is being upgrade while the MCU is also transferring data. R2 is also a 2.2KΩ resistor, it can be changed to 0Ω.

A reference firmware upgrade operation procedure is listed below:

1. Power off the module.
2. Connect the upgrade board to the UART of PC and the 4-pin connector when the module needs firmware upgrade..
3. Press the Start button in the firmware upgrade tool in PC. (Note: The firmware upgrade tool will send download synchronization code to the UART port of the module, and wait for the acknowledgement from the module.)
4. Power on the module.
5. The module will automatically enter firmware upgrade procedure.

Please refer to the chapter 3.1 about level shifter

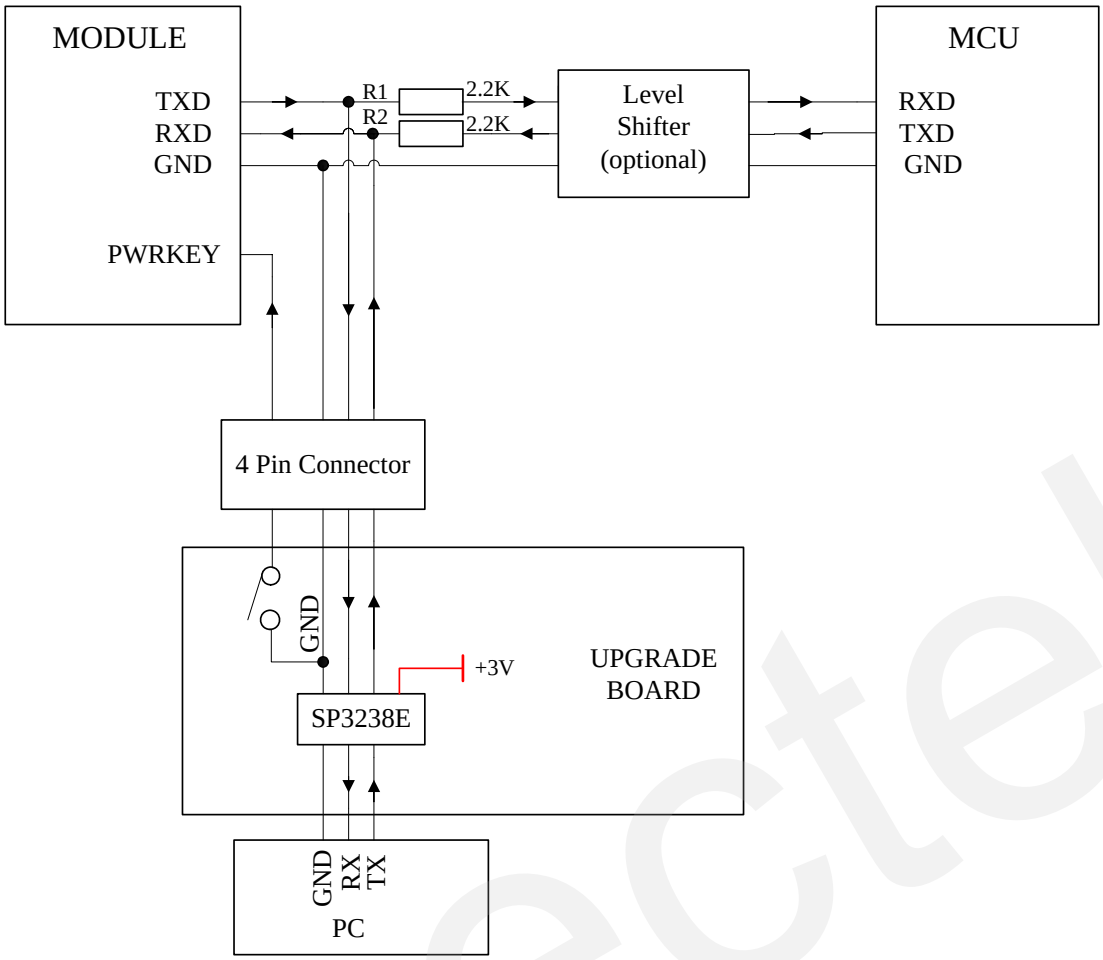

Figure 6: The connection for firmware upgrade

5. Flow control

Flow control is essential to prevent loss of data or avoid errors when, in a data or fax call, the sending device is transferring data faster than the receiving side is ready to accept. When the receiving buffer reaches its capacity, the receiving device should be capable to cause the sending device to pause until it catches up.

There are basically two approaches to achieve data flow control: software flow control and hardware flow control.

5.1. Software flow control (XON/XOFF flow control)

Software flow control sends different characters to stop (XOFF, decimal 19) and resume (XON, decimal 17) data flow. It is quite useful in some applications that only use three wires on the serial interface.

The default flow control approach of the module is hardware flow control (RTS/CTS flow control). To enable software flow control in the DTE interface and within GSM engine, type the following AT command:

AT+IFC=1, 1

This setting is stored volatile. In order to keep this configuration, AT&W should be executed to save the configuration in the user profile.

Ensure that any communication software package (e.g. ProComm Plus, Hyper Terminal or WinFax Pro) uses software flow control.

NOTE:
Software Flow control should not be used for data calls where binary data will be transmitted or received (e.g. TCP/IP) as the DTE interface may interpret binary data as flow control characters.

5.2. Hardware flow control (RTS/CTS flow control)

Hardware flow control achieves the data flow control by controlling the RTS/CTS line. When the data transfer should be suspended, the CTS line is set inactive until the transfer from the receiving buffer has completed. When the receiving buffer is ok to receive more data, CTS goes active once again.

To achieve hardware flow control, ensure that the RTS/CTS lines are present on your application platform.

6. Control Signals

6.1. DCD

The DCD pin will be active (low) after establishing a data connection. When the data connection is turned off, the DCD pin will go to inactive (high)

6.2. DTR

The module would automatically go into SLEEP mode, if the DTR is set to high level, the slow clocking mode is already enabled by AT+QSCLK, and there is no specific task for the module to handle. In this case, the current consumption of module will reduce to the minimal level. During the SLEEP mode, the module can still receive paging message and SMS normally. If the DTR Pin is pulled down, the module would exit from SLEEP mode. The UART port will be active about 600ms after the DTR is changed to low level.

DTE can use the DTR pin to control the active or inactive state of the SLEEP mode as shown in Figure 7.

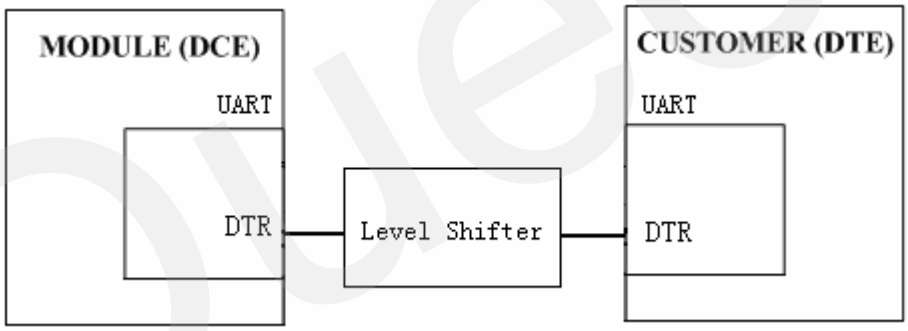

Figure 7: DTR for waking up

In TCP/IP application (for more detail, please refer to TCP/IP application notes), the DTR pin can also be used to switch from data mode to command mode. To use this method, AT&D1 should be set firstly. Depending on the state of the DTR pin, there are 2 ways to implement this function.

1. If the DTR pin is set to low in data mode, setting it to high for about 600ms would force the UART port from data mode to command mode.
2. If the DTR pin is set to high in data mode, pulling it to low level for about 1000ms and then pulling it up for about 600ms would also switch the module from data mode to command mode.

When the module successfully switches from data mode to command mode, a URC “OK” will be

returned to indicate the command mode.
Note: AT&D1 is volatile. Executing AT&W to save this profile if necessary.

6.3. RI

If the module acts as a caller, the RI pin would keep to high. On the other hand, if the module acts as a receiver, the responses of RI pin in different situations are listed in Table 3.

Table 3: RI responses

State	RI respond
Standby	HIGH
In-coming voice call ringing	Change to LOW, then: (1) Change to HIGH after establishing a voice call. (2) Change to HIGH when using command ATH to reject the calling. (3) Change to HIGH when caller hangs up the call.
Data calling	Change to LOW, then： (1) Change to HIGH after establishing a data call. (2) Change to HIGH when using command ATH to reject the data calling. (3) Change to HIGH when caller hangs up the data calling.
SMS	The RI will change to LOW and hold low level for about 120 ms, then change to HIGH.
URC	The following URC messages trigger a low level that lasting 120ms on RI pin UNDER-VOLTAGE WARNNING OVER-VOLTAGE WARNNING RING Call Ready +CMTI： +CMT： +TSMSINFO: +CDS:

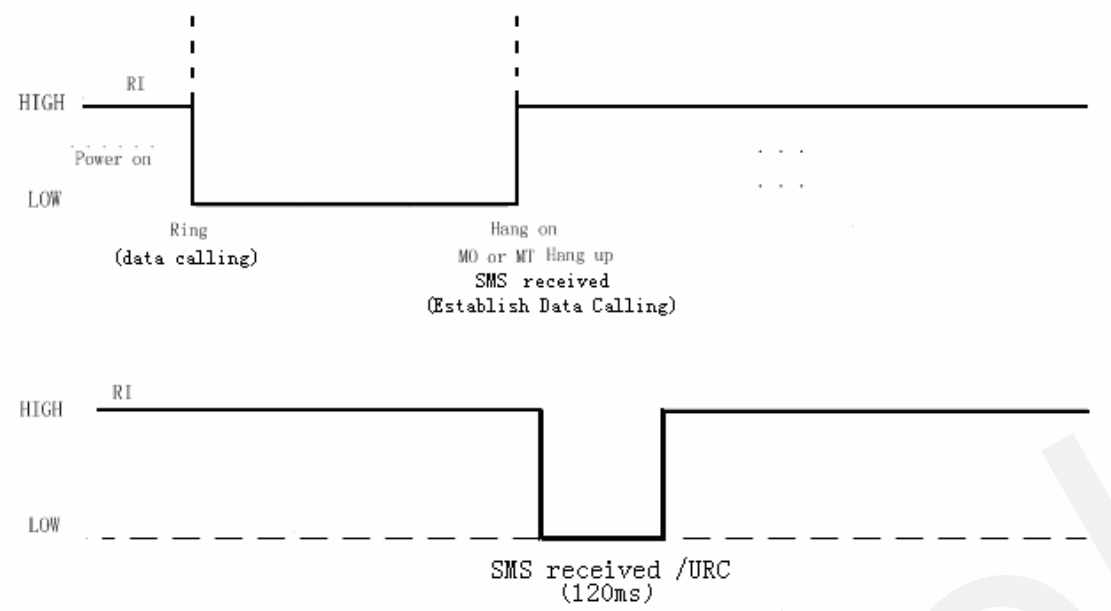

Figure 8: Behaviours of RI

Table 4: AT+QINDRI Indicates RI when using URC

AT command	Response	Parameter
Read command AT+ QINDRI?	+QINDRI: <status> Ok	See set command
Set Command AT+ QINDRI=<status>	OK	<status> 0 on 1 off

It is recommended to connect the RI pin to an interrupt pin of Host MCU, as the RI indication can be used to wake up the MCU from power saving mode.

Shanghai Quectel Wireless Solutions Co., Ltd.

Room 801, Building E, No.1618, Yishan Road, Shanghai, China 201103

Tel: +86 21 5108 2965

Mail: info@quectel.com